REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-5 remain pending in the application.

Claim 2 is objected to because of the noted informalities. In response, claim 2 has been amended to overcome this objection.

Claim 1 is rejected under 35 USC §103(a) as being unpatentable over Kamimura et al. ('565) and further in view of Kub ('604). In response, claim 1 has been amended and is believed to be patentable over this combination of references for the reasons discussed below.

Basically, the invention proposes a new manner of forming a very small reading diode for receiving charges from a register. The reading diode should be very small so as to have a small capacitance, in order to be able to operate reading of charges at a high speed. The context in which use of the invention is envisaged is that of a CCD reading register (mainly for an image sensor).

The reading diode is adjacent to two silicon electrodes which serve to open or close potential barriers for allowing transfer of the charges to be read. One silicon electrode is intended for allowing charges into the reading diode; the other silicon electrode is intended for allowing removal of charges out of the reading diode.

Claim 1 has been amended to clarify the fact that the invention is intended for building the reading diode of a CCD register.

Concerning the rejection of claim 1, the Examiner indicates that Kamimura '565 discloses the claimed process except for thermally oxidizing the electrodes, and that Kub '604 discloses oxidizing electrodes to form an insulating layer, thus showing that thermal oxidation would have been an option in Kamimura as well. It is, however, respectfully submitted that it would have been unacceptable for the skilled in the art to provide insulating layer 6 as a thermal insulation because either the resulting thermal

oxide would have been thin and, then, an unacceptably high capacitance would appear between conductive layer 7 and the register, or the resulting insulating layer would be thick and then, as is well known for thermal oxidation, the electrodes would have disappeared, being consumed by the oxidation.

Note that although Kub discloses thermal oxidation to provide separation between adjacent electrodes of the register, Kub does not provide similar insulation to insulate the last electrode from conductive connection 44, which obviously shows that the skilled in the art does not use thermal oxidation in any instance to replace non thermal oxidation, and particularly not for a contact on a diode adjacent a register electrode. Note that conductive connection 44 of Kub is not a contact with a reading diode. Rather it is a contact for a separation channel between two channels. The problem of reducing the reading diode size is not relevant in Kub. It is respectfully submitted that Kamimura '565 and Kub '604 would not be combined in the manner suggested by the Examiner. Accordingly, the obviousness rejection of claim 1 should be withdrawn.

Claim 2 is rejected under 35 USC §103(a) as being unpatentable over Kamimura et al. ('565) and Kub ('604) and further in view of Zoroglu ('535). Applicant respectfully traverses this rejection.

Claim 2 is dependent upon claim 1, and recites additional, important limitations and should be patentable for the reasons discussed above with respect to claim 1 as well as on its own merits. Accordingly, the obviousness rejection should be withdrawn.

Claim 3 is rejected under 35 USC §103(a) as being unpatentable over Kamimura et al. ('565), Kub ('604), Zoroglu ('535) and further in view of Wolf (Silicon Processing for for the VLSI Era, page 331). Applicant respectfully traverses this rejection.

Claim 3 is dependent upon claim 1, and recites additional, important limitations and should be patentable for the reasons discussed above with respect to claim 1 as well as on its own merits. Accordingly, the obviousness rejection should be withdrawn.

Claim 4 is rejected under 35 USC §103(a) as being unpatentable over Stevens ('990) et al. ('565) and further in view of Kamimura ('565). In response, claim 4 has been amended and is believed to be patentable over this combination of references for the reasons discussed below.

In the commonly used CCD technology, the reading diode is made by forming an impurity diffusion (for instance let us assume N type impurities into a P substrate) in a small aperture between the two silicon electrodes, and an aluminum deposition in the aperture, in direct contact with the N-type diffusion. This is what is shown in Stevens '990 cited in the Office action against claims 4 and 5.

The Examiner indicates that claim 4 is obvious over Stevens '990 in view of Kamimura '565. Stevens '990, as indicated by the Examiner does not disclose the original feature of the invention, i.e., the fact that no aluminum contact is taken into the diode region, in order to allow the diode region to be smaller than it would be if it had an aluminum contact. The inventor in the instant application has recognized that, although an aluminum contact may be made small, it still requires a minimum surface dictated by so-called rules of design of integrated circuits and it would be useful to still reduce it. The invention as claimed in claim 1 and 4 allows such a reduction.

The Examiner indicates that Kamimura '565 teaches what Stevens '990 does not teach.

However, it is respectfully submitted that Kamimura '565 shows a structure which is significantly different from that which is claimed and does not help suggesting the invention. The teachings of Kamimura '565 do not relate in any way to the manufacturing of the reading diode of a CCD register. The teachings of Kamimura relate to the manufacturing of a three layer amorphous photoconductive layer. Kamimura '565 does illustrate an embodiment where a deported contact with a diode (but not the reading diode of the register) is used. Applicant recognizes that deported contacts in a way exist in a number of integrated circuits since conductive layers generally serve to establish contacts between zones apart from each other; however,

deported contacts are not used when there is apparently no reason to deport a contact; there is no showing or suggestion in the prior art, whether Stevens '990 or Kamimura '565, that a deported contact could be a way to permit critical reduction of size of a CCD reading diode under the dimension of a minimum surface required for an aluminum contact.

Kamimura provides teachings about the three layer amorphous photoconductive layer. The structure that appears in figure 1 under the three layer photoconductive layer is shown only for illustrative purpose. Assuming Kamimura '565 would also provide clear secondary teachings on the illustrative structure shown in figure 1, there is no constraint of size of the diode (not a reading diode) and no constraint of having a size smaller than what an aluminum contact would allow, since Kamimura '565 explicitely indicates that the contact on the N+ diffusion could be aluminum (Al-Si).

What the skilled in the art could derive from the Kamimura '565 structure would probably be the following: layers 7 and 9 laterally extend over the shift register 3 because they help to mask the register from light since a register is intrinsically affected by light and this phenomenon is undesired in a shift register. This teaching is however no teaching relative to a way of reduction of size of a reading diode in a CCD register.

Therefore, there is no motivation for the skilled in the art to incorporate the secondary teachings of Kamimura into Stevens; not only because the main teachings of Kamimura relate to the three layer amorphous silicon over the device but also because no possible teaching can be derived from Kamimura '565 relative to a way of reducing a diode size, and more specifically a reading diode size, down to below what an aluminum contact could allow.

In addition to that, it is respectfully submitted that the question of the size of the diode in Kamimura '565 is not considered and would not be considered by the skilled in the art who is concerned with the question of speed of transfer: the typical available transfer time in the structure of Kamimura is much higher than the typical available time for a reading diode. Typically, in an image sensor having 1000 lines and 1000 colonnes,

the available transfer time within a column is 1000 times the available transfer time within the reading register. Therefore, it is very unlikely that a person skilled in the art would indirectly derive from Kamimura '565 unwritten teachings about the question of speed of transfer or size of the illustrative diode, and very unlikely that he would think of adapting any secondary teaching of Kamimura to his speed problem. Accordingly, the obviousness rejection should be withdrawn.

Claim 5 is rejected under 35 USC §103(a) as being unpatentable over Stevens ('990) Kamimura et al. ('565) and further in view of Spangler et al. ('064). In response, claim 5 has been amended and is believed patentable over this combination of references for the reasons discussed below.

Turning to the rejection of claim 5, it is respectfully submitted that use of silicon nitride is common in the semiconductor industry, and Sprangler '064 only confirms that general statement; however silicon nitride is not suggested in the configuration which is defined in claim 4 for a reading diode of a CCD register, because layer 18 is sufficient to provide the insulation and protection against impurities that the Examiner mentions as being motivation for using silicon nitride. Claim 5 is amended to specify the feature that the silicon nitride has the same pattern as the etched polycrystalline silicon layer.

Further, claim 5 is dependent upon claim 4 and should be patentable for the reasons discussed above with respect to claim 4 as well as on its own merits. Accordingly, the obviousness rejection should be withdrawn.

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

Early issuance of a Notice of Allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

Application No.: 10/591,178 **Docket No.: 4590-556**

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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